In The Claims:

Claims 1-60 (canceled)

61. (previously presented) A chip packaging method comprising:

providing a bulk metal substrate without conductive traces;

providing a plurality of dies, wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads located on the active surface;

mounting the dies onto the bulk metal substrate, the backside of the dies facing the bulk metal substrate; and

forming a plurality of patterned lines over the active surface of the dies, wherein the patterned lines are constructed from at least a patterned wiring layer.

62. (original) The method of claim 61, wherein the dies perform same functions.

63. (original) The method of claim 61, wherein the dies perform different functions.

Claims 64-66 (canceled)

67. (previously presented) The method of claim 61, wherein the bulk metal substrate comprises a first metal layer and a second metal layer, the first metal layer is mounted on the second layer, the first metal layer has a plurality of openings that penetrate through the first metal layer and expose the second metal layer to form a plurality of cavities, the backside of the dies is mounted on the second metal layer, and the patterned lines formed over the second metal layer..

68. (original) The method of claim 67, wherein a thickness of the first metal layer is approximately equal to a thickness of the dies.

69. (previously presented) The method of claim 67, wherein the steps of forming the metal layer comprise:

punching the first metal layer to form the openings that penetrate through the first metal layer; and

overlapping the first metal layer and the second metal layer.

Claims 70-71 (canceled)

72. (previously presented) The method of claim 61, further comprising forming a dielectric layer over the active surface of the dies after mounting the dies onto the bulk metal substrate and before forming the patterned lines over the active surface of the dies.

73. (previously presented) The method of claim 72, wherein a material of the dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

74. (previously presented) The method of claim 61, further comprising forming a dielectric layer over the patterned lines after forming the patterned lines over the active surface of the dies.

75. (previously presented) The method of claim 74, wherein a material of the dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

76. (previously presented) The method of claim 61, wherein the step of forming the patterned lines over the active surface of the dies is provided by a technology compsising electroplating.

77. (previously presented) The method of claim 61, wherein the step of forming the patterned lines over the active surface of the dies is provided by a technology compsising sputtering and electroplating.

78. (previously presented) The method of claim 61, further comprising depositing a plurality of bonding points on a plurality of bonding pads of the patterned lines after forming the patterned lines over the active surface of the dies.

79. (previously presented) The method of claim 78, wherein the bonding points comprise solder balls.

80. (previously presented) The method of claim 61, further comprising performing a singularizing process to form a plurality of chip package structures after forming the patterned lines over the active surface of the dies.

81. (previously presented) The method of claim 80, wherein each chip package structure has a single die.

82. (previously presented) The method of claim 80, wherein each chip package structure has a plurality of dies.

83. (previously presented) The method of claim 61, wherein the step of forming the patterned lines over the active surface of the dies comprises forming a single patterned wiring layer.

84. (previously presented) The method of claim 61, wherein the step of forming the patterned lines over the active surface of the dies comprises forming a plurality of patterned

wiring layers and at least a dielectric layer, the dielectric layer formed between the patterned wiring layers.

85. (previously presented) The method of claim 84, wherein a material of the dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

86. (previously presented) The method of claim 61, wherein the step of forming the patterned lines over the active surface of the dies comprises forming a passive device over the active surface of the dies.

87. (previously presented) The method of claim 86, wherein the passive device comprises a capacitor.

88. (previously presented) The method of claim 86, wherein the passive device comprises a resistor.

89. (previously presented) The method of claim 86, wherein the passive device comprises an inductor.

90. (previously presented) The method of claim 86, wherein the passive device comprises a wave-guide.

91. (previously presented) The method of claim 86, wherein the passive device comprises a filter.

92. (previously presented) The method of claim 86, wherein the passive device comprises a micro electronic mechanical sensor (MEMS).

93. (previously presented) The method of claim 61, wherein the bulk metal substrate is constructed from copper.

94. (previously presented) The method of claim 61, wherein the bulk metal substrate is constructed from aluminum alloy.

Claims 95-138 (canceled)

Application No.: 10/055,560 **Docket No.: JCLA8532**

No new matter adds through the amendments. Entry of the amendment is requested. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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